What is claimed is:

1. A semiconductor device, comprising:

a gate electrode formed on a substrate through a gate insulating film lying therebetween;

first and second diffused layers formed opposite to each other across the portion of the substrate existing under the gate electrode and having a first conduction type, each having a second conduction type different from the first conduction type of the portion;

a wiring layer formed above the gate electrode; and

a contact formed within a contact hole between the wiring layer and the substrate, which connects the wiring layer to the first diffused layer and the gate electrode.

2. A semiconductor device according to claim 1, wherein the contact is connected also to the second diffused layer.

3. A semiconductor device according to claim 1, comprising:

a third diffused layer formed on the substrate; and

an isolation area formed between the first and the third diffused layers, which separates the first and the third diffused layers each other;

wherein the contact is connected further to the third diffused layer.

4. A semiconductor device, comprising:

a gate electrode formed on a substrate through a gate insulating film;

a diffused layer formed on the substrate;

a wiring layer formed above the gate electrode; and

a contact formed within a contact hole between the wiring layer and the substrate, which connects the wiring layer to the diffused layers and the gate electrode,

wherein the diffused layer has first and second portions formed opposite to each other across the portion of the substrate existing under the gate electrode and having a first conduction type, each having a second conduction type different from the first conduction type of the portion of the substrate; and a third portion that connects the first portion to the second portion.

5. A semiconductor device according to claim 4, wherein the contact is connected to the first portion and the second portion of the diffused layer.

6. A semiconductor device according to claim 4, comprising:

another diffused layer formed on the substrate; and

an isolation area formed between the diffused layer and the other diffused layer, which separates the diffused layer and the other diffused layer, wherein the contact is connected further to the other diffused layer.

7. A semiconductor device according to claim 1, comprising a SRAM cell, wherein the wiring layer is connected

to the memory node of the SRAM cell.

8. A semiconductor device according to claim 1, comprising a bistable trigger circuit, wherein the wiring layer is connected to the memory node of the bistable trigger circuit.

9. A semiconductor device according to claim 1, comprising: another gate electrode formed on the substrate through another gate insulating film, and a transistor for composing a semiconductor integrated circuit therein, wherein the film thickness of the gate insulating film is thinner than the one of the other gate insulating film.

10. A semiconductor device according to claim 1, comprising another gate electrode formed on the substrate through another gate insulating film, and a transistor for composing a semiconductor IC therein, wherein the relative dielectric constant of the gate insulating film is higher than the one of the other gate insulating film.

11. A semiconductor device according to claim 1, comprising a source area and a drain area formed opposed to each other across the channel portion of the substrate existing under the gate electrode, and a transistor for composing a semiconductor IC therein, wherein the impurity concentrations of the first diffused layer and the second diffused layer are higher than the ones of the source and the drain areas.

12. A semiconductor device according to claim 4, comprising a source area and a drain area formed opposed to each

other across the channel portion of the substrate existing under the gate electrode, and a transistor for composing a semiconductor IC therein, wherein the impurity concentration of the diffused layer is higher than the impurity concentration s of the source area and the drain area.

13. A semiconductor device according to claim 1 or claim 4, comprising a SRAM cell, wherein the wiring layer is connected to the memory node of the SRAM cell.

14. A semiconductor device according to claim 4, comprising a bistable trigger circuit, wherein the wiring layer is connected to the memory node of the bistable trigger circuit.

15. A semiconductor device according to claim 4, comprising: another gate electrode formed on the substrate through another gate insulating film, and a transistor for composing a semiconductor integrated circuit therein, wherein the film thickness of the gate insulating film is thinner than the one of the other gate insulating film.

16. A semiconductor device according to claim 4, comprising another gate electrode formed on the substrate through another gate insulating film, and a transistor for composing a semiconductor IC therein, wherein the relative dielectric constant of the gate insulating film is higher than the one of the other gate insulating film.